REMARKS

Claims 1-17 are pending in the application. Claims 1-12 and 14 have been withdrawn from consideration. Claims 13 and 15-17 have been rejected.

Objection to the Title

The Examiner asserts that the title of the invention is not descriptive. A new title is provided, as required by the Examiner.

Claim Rejections under 35 USC §102

Claims 13 and 15-17 stand rejected under 35 U.S.C. §102(b) as being anticipated by Gorczyca (U.S. 5,492,586).

The present invention is an electronic parts packaging structure in which five embodiments are described in the specification. Claims 13 and 15-17 which are currently being prosecuted are directed to the first embodiment as illustrated in Figures 2A-2H. The first embodiment includes, as shown in Figure 2A, a base substrate (24) on which a wiring substrate is prepared. Through-holes (24a) are provided in the base substrate (24) and through-hole plating layers (24b) are connected to a first wiring patterns (28). A first interlayer insulation film (30) is placed on top of the first wiring patterns (28). First via holes (30x) are formed on the first interlayer insulation film (30). A second wiring patterns (28a) is formed on the first interlayer insulation film (30). As shown in Figure 2B, a first resin film (32a) is formed on the second wiring patterns (28a) and the first interlayer insulation

film (30). As shown in Figure 2C, a semiconductor chip (20) (electronic parts)is embedded in the first resin film (32a). Connection pads (21a) (connection terminals) are exposed on the element formation surface of the semiconductor chip (20). As shown in Figure 2D, a second interlayer insulation film (32) is created composed of the first resin film 32a (first insulating film) and a second resin film (32b) (second insulation film). As shown in Figure 2E, via holes (32x) are formed in the second interlayer insulation film (32) on the connection pads (21a) of the semiconductor chip (20) and on the second wiring patterns (28a). As shown in Figure 2G, a third wiring patterns (28b) (upper wiring patterns) are connected to the connection pads (21a) of the semiconductor chip (20) and to the second wiring patterns (28a) through the second via holes (32x), formed on the second interlayer insulation film (32). Finally, an upper semiconductor chip (20x) (upper electronic parts) with bumps (23) which are flip-chip bonded to the connection portions (28z) of the third wiring patterns (28b).

Gorczyca describes a method for fabricating a multi-chip module substrate. This module includes a base (24) that supports a base sheet (14) on which a carrier (10) is attached. A protective dielectric layer (16) is applied to the carrier (10). As illustrated in Figure 11 is a view of a plurality of vias (30) and electrically conductive interconnections (32) through a laminatable dielectric layer (26). As illustrated in Figure. 12 back vias (34) are shown along with electrically conductive thermal paths (36) for chip backsides. As shown in Figure 13, a chip (20) is embedded in laminatable dielectric layer (26).

In amended Claim 13, an upper surface of the second insulation film for covering the electronic parts is flat over a whole on the wiring substrate. And an upper electronic parts is flip-

chip bonded to the upper wiring pattern which is formed as a single layer and directly contacts the upper surface of the second insulating film.

By this matter, the electronic parts is buried in the first insulation film in the state where steps due to the thickness of the electronic parts are eliminated. Since the upper surface of the second insulation film is flat over a hole on the wiring substrate, the electronic parts can be flip-chip bonded to the wiring pattern with high reliability, and making electronic parts packing structure thin type and high density type becomes possible.

In Gorczyca, it is not considered that the upper electronic parts are flip-chip bonded above the chip 20. Also, the upper surface of the protective dielectric layer 16 covering the chip 20 is not flat over a whole of the base 24. Therefore, Claims 13, as amended , further distinguishes over the prior art. Therefore, withdrawal of the rejection of claims 13 and 15-17 under 35 U.S.C. §102(b) as being anticipated by Gorczyca (U.S. 5,492,586) is respectfully requested.

Claim Rejections under 35 USC §103

Claims 13 and 15-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eichelberger (U.S. 5,111,278).

Eichelberger describes a multichip integrated circuit package. The multichip module (20) includes a substrate base (30) with metalized via holes (32). The IC chips (38) are encapsulated in a polymer material (42) and connections (43) are provided from the conductors under the chips to conductors (44) over the chips.

In Eichelberger (FIG. 2), the multi-layer wiring patterns 44, 46 formed above the chip 38 are indicated, and it is not described that an upper electronic part is flip-chip bonded to the wiring pattern 44 as a single layer which directly contacts the upper surface of the insulating film 42 covering the chip 38.

Therefore, Claims 13, as amended , further distinguishes over the prior art. Therefore, withdrawal of the rejection of claims 13 and 15-17 under 35 U.S.C. §103(a) as being unpatentable over Eichelberger (U.S. 5,111,278) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 13 and 15-17, as amended, are believed to be patentable and in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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